AMENDMENT TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

1. (currently amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity [[over]] on the surface of said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance.

2. (original) The method of claim 1 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

3. (currently amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity on the surface of said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer,

wherein said contact layer has a second resistance lower than said first resistance, and ~~The method of claim 1~~ wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

4. (original) The method of claim 3 wherein said exposure is conducted for about 100-130 seconds using a plasma chemical vapor deposition apparatus.

5. (currently amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity on the surface of said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and ~~The method of claim 1~~ wherein said diffusion of said impurity into said contact [[region]] portion is performed by heat annealing.

6. (original) The method of claim 5 wherein said heat annealing is conducted at a temperature of about 300°C - 320°C for about 10-15 minutes.

7. (original) The method of claim 1 wherein said impurity is phosphorus.

8. (original) The method of claim 1 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

9. (original) The method of claim 1 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

10. (canceled)

11. (previously presented) The method of claim 1 wherein said silicon layer is etched utilizing a common photoresist to form said electrodes.

12. (original) The method of claim 1 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

13. (currently amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity;

etching said silicon layer utilizing a common photoresist to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance.

14. (original) The method of claim 13 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

15. (original) The method of claim 13 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

16. (original) The method of claim 15 wherein said exposure is conducted for about 100 - 130 seconds using a plasma chemical vapor deposition apparatus.

17. (original) The method of claim 13 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

18. (original) The method of claim 17 wherein said heat annealing is conducted at a temperature of about 300°C - 320°C for about 10 - 15 minutes.

19. (original) The method of claim 13 wherein said impurity is phosphorus.

20. (original) The method of claim 13 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

21. (original) The method of claim 13 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

22. (canceled)

23. (original) The method of claim 13 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

24. (currently amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity [[over]] on the surface of said amorphous silicon layer;

providing a photoresist over said impurity and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

subsequently, removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance, and wherein essentially none of said impurity is diffused into said contact portion prior to said removing step.

25. (original) The method of claim 24 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

26. (original) The method of claim 24 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

27. (original) The method of claim 26 wherein said exposure is conducted for about 100 - 130 seconds using a plasma chemical vapor deposition apparatus.

28. (original) The method of claim 24 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

29. (original) The method of claim 28 wherein said heat annealing is conducted at a temperature of about 300°C - 320°C for about 10-15 minutes.

30. (original) The method of claim 24 wherein said impurity is phosphorus.

31. (original) The method of claim 24 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

32. (original) The method of claim 24 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

33. (canceled).

34. (original) The method of claim 24 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

35. (withdrawn) A thin film transistor comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

36. (withdrawn) The transistor of claim 35 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

37. (withdrawn) The transistor of claim 35 wherein said impurity is phosphorus.

38. (withdrawn) The transistor of claim 35 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

39. (withdrawn) The transistor of claim 35 wherein said silicon layer is amorphous.

40. (withdrawn) A thin film transistor comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer; wherein said silicon layer is etched utilizing a common photoresist used to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

41. (withdrawn) The transistor of claim 40 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

42. (withdrawn) The transistor of claim 40 wherein said impurity is phosphorus.

43. (withdrawn) The transistor of claim 40 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

44. (withdrawn) The transistor of claim 40 wherein said silicon layer is amorphous.

45. (withdrawn) A thin film transistor comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon wherein said channel region is formed by providing a photoresist over said impurity provided silicon layer and back exposing said photoresist utilizing said gate as a mask and developing a pattern substantially identical with that of said gate and removing said pattern; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

46. (withdrawn) The transistor of claim 45 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

47. (withdrawn) The transistor of claim 45 wherein said impurity is phosphorus.

48. (withdrawn) The transistor of claim 45 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

49. (withdrawn) The transistor of claim 45 wherein said silicon layer is amorphous.

50. (currently amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity [[over]] on the surface of said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance.

51. (original) The method of claim 50 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

52. (original) The method of claim 50 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

53. (original) The method of claim 52 wherein said exposure is conducted for about 100-130 seconds using a plasma chemical vapor deposition apparatus.

54. (original) The method of claim 50 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

55. (original) The method of claim 54 wherein said heat annealing is conducted at a temperature of about 300°C - 320°C for about 10-15 minutes.

56. (original) The method of claim 50 wherein said impurity is phosphorus.

57. (original) The method of claim 50 wherein said amorphous silicon film is deposited to a thickness of about 150 nm — 200 nm.

58. (original) The method of claim 50 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

59. (canceled).

60. (original) The method of claim 50 wherein said silicon layer is etched utilizing a common photoresist used to formed said electrodes.

61. (original) The method of claim 50 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

62. (currently amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity [[over]] <u>on the surface of</u> said amorphous silicon layer, <u>wherein said impurity does not diffuse into said amorphous silicon layer</u>;

etching said amorphous silicon layer utilizing a common photoresist to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and then diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance.

63. (original) The method of claim 62 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

64. (original) The method of claim 62 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

65. (original) The method of claim 64 wherein said exposure is conducted for about 100 - 130 seconds using a plasma chemical vapor deposition apparatus.

66. (original) The method of claim 62 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

67. (original) The method of claim 66 wherein said heat annealing is conducted at a temperature of about 300°C - 320°C for about 10 - 15 minutes.

68. (original) The method of claim 62 wherein said impurity is phosphorus.

69. (original) The method of claim 62 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

70. (original) The method of claim 62 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

71. (canceled).

72. (original) The method of claim 62 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

73. (currently amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity;

providing a photoresist over said impurity and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance.

74. (original) The method of claim 73 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

75. (original) The method of claim 73 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

76. (original) The method of claim 75 wherein said exposure is conducted for about 100-130 seconds using a plasma chemical vapor deposition apparatus.

77. (original) The method of claim 73 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

78. (original) The method of claim 77 wherein said heat annealing is conducted at a temperature of about 300°C - 320°C for about 10-15 minutes.

79. (original) The method of claim 73 wherein said impurity is phosphorus.

80. (original) The method of claim 73 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

81. (original) The method of claim 73 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

82. (canceled).

83. (original) The method of claim 73 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

84. (withdrawn) A liquid crystal display device comprising:

a plurality of thin film transistors provided on a LCD substrate in a matrix form, each of said thin film transistors comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

85. (withdrawn) The device of claim 84 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

86. (withdrawn) The device of claim 84 wherein said impurity is phosphorus.

87. (withdrawn) The device of claim 84 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

88. (withdrawn) The device of claim 84 wherein said silicon layer is amorphous.

89. (withdrawn) A liquid crystal display device comprising:

a plurality of thin film transistors provided on a LCD substrate in a matrix form, each of said thin film transistors comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

wherein said silicon layer is etched utilizing a common photoresist used to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

90. (withdrawn) The device of claim 89 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

91. (withdrawn) The device of claim 89 wherein said impurity is phosphorus.

92. (withdrawn) The device of claim 89 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

93. (withdrawn) The device of claim 89 wherein said silicon layer is amorphous.

94. (withdrawn) A liquid crystal display device comprising:

a plurality of thin film transistors provided on a LCD substrate in a matrix form, each of said thin film transistors comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon wherein said channel region is formed by providing a photoresist over said impurity provided silicon layer and back exposing said photoresist utilizing said gate as a mask and developing a pattern substantially identical with that of said gate and removing said pattern; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

95. (withdrawn) The device of claim 94 wherein said contact layer contains a concentration of said impurity of at least 0.01 %.

96. (withdrawn) The device of claim 94 wherein said impurity is phosphorus.

97. (withdrawn) The device of claim 94 wherein said amorphous silicon film is deposited to a thickness of about 150 nm - 200 nm.

98. (withdrawn) The device of claim 94 wherein said silicon layer is amorphous.